

# FLIP-FLOPS

## Objectives:

1. To become familiar with flip-flops.
2. To implement and observe the operation of different flip-flops.

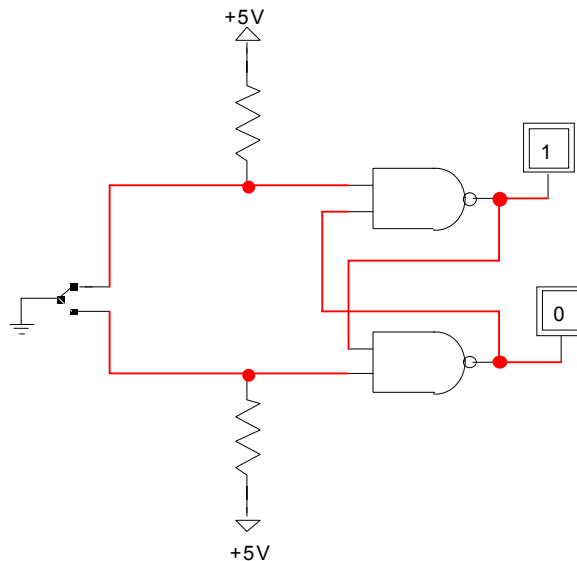
## Apparatus:

- IC type 7400 quad 2-input NAND gate
- IC type 7410 triple 3- input NAND gate
- IC type 7476 dual JK master-slave flip-flops.
- IC type 7474 dual D positive-edge-triggered flip-flops.
- Dual trace oscilloscope.

Theory: See sections 6-2 and 6-3 of your text.

## Procedure:

1. In the pre-lab using LogicWorks construct the circuit shown in Fig.1



Where we could use generic NAND gates or 74-00 and Binary Probes to simulate LEDs. Finally, we use SPDT for the bouncing switch. Using the simulated circuit fill in the truth table.

S	R	Q	Q'
1	0		
1	1		
0	1		
1	1		
0	0		

In the Lab, Build the RS latch shown in fig.2. Use SPDT switch S2 as a bouncing switch. Q and Q' Outputs are connected to LED'S of the PB-503. Verify the truth table experimentally.

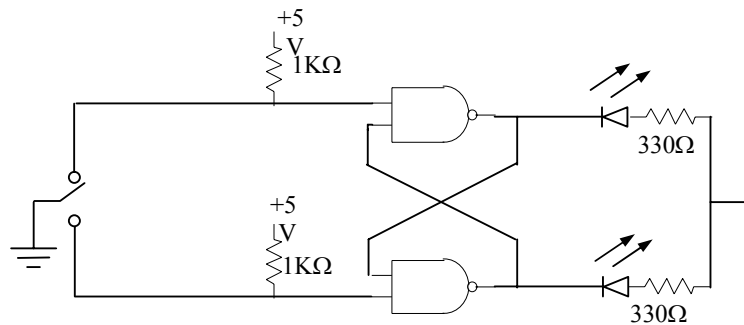


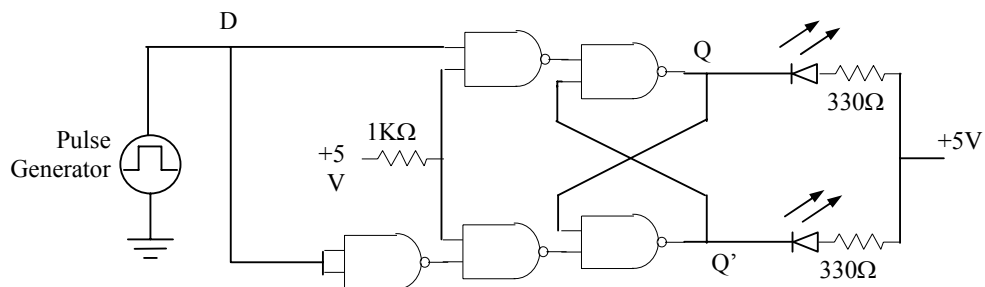
Fig. 2

2. Modify the basic R-S into a D latch by adding the steering gates and the inverter shown in Fig 3.

Connect the D input to the pulse generator of the digi designer and set it at 1 Hz.

Connect the enable input to a high through 1k resistor. Observe the output; obtain the truth table experimentally then change the enable to a low.

Is the enable an active high or an active? Leave the enable low and place a momentary short to ground first on one output and then on the other. What happens?



3. The 7476 is a dual JK master-slave flip-flops with preset and clear inputs. The function table given in table 1 defines the operation of the flip-flop. The +ve transition of the CLOCK (CP) pulse changes the master flip-flop, and the (-ve) transition of the CLOCK (CP) pulse changes the slave flip-flop.

transition changes the slave flip-flop as well as the output of the circuit. In LogicWorks the chip 7476 is not available, however, the generic JK flip-flop behave in exactly the same way as the 7476. The “S” represents the Preset, the “R” represents the Clear, and C represents the clock pulse (CP). Verify the table by connecting Binary switches to R, S, J, K, and C. Notice that only the negative edge of the clock affects the outputs (Q, and Q’).

Table 1

Input					Output	
Preset	Clear	Clock	J	K	Q	Q'
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1	1
1	1		0	0	No change	
1	1		0	1	0	1
1	1		1	0	1	0
1	1		1	1	Toggle	

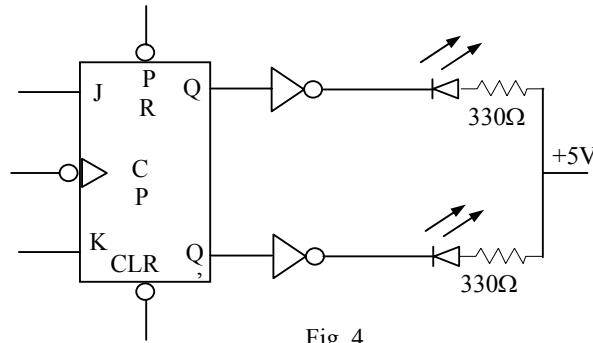


Fig. 4

In the Lab, Construct the circuit of Fig 4. Look at the data sheet for the 7476 and determine the inactive logic required at the PRE and CLR inputs.

Connect the 7476 for the SET mode by connecting J = 1, K = 0. With CLOCK (CP) = 0; test the effect of PRE, CLR by putting a 0 on each, one at a time.

Put CLR = 0, then pulse the clock (CP) by putting a HIGH then a LOW, on the clock. Does the CLR input override J input?

Verify the operation of the JK flip flop by experimentally obtaining the characteristic table.

